Confirmation No. 8431

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	TERECHKO, *et al.*	Examiner:	Bae, Ji. H.
Serial No.:	10/561,627	Group Art Unit:	2115
Filed:	December 19, 2005	Docket No.:	NL021504US
Title:	REGISTER FILE GATING TO REDUCE MICROPROCESSOR POWER DISSIPATION		

BRIEF ON APPEAL

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed April 21, 2008 and in response to the rejections of claims 1-21 as set forth in the Final Office Action dated December 21, 2007 and in acknowledgment of the Advisory Action dated March 19, 2008.

Please charge Deposit Account number 50-0996 (NXPS.306PA) $510.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017402/0022 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application have been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-21 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments to claims 1-10 and 12-21 have been filed subsequent to the Final Office Action dated December 21, 2007. An amendment to claim 14 was filed on June 13, 2008, per discussion with Examiner Bae; the listing of claims in the Appendix reflects this amendment.

V. Summary of Claimed Subject Matter

According to an example embodiment and as generally consistent with claim 1, a circuit arrangement includes a register file (*see, e.g.*, 60 in FIG. 2 and paragraph 0037) and enable logic (*see, e.g.*, 62 in FIG. 2, 82 in FIG. 3 and paragraphs 0037, 0058) coupled to the register file. The register file is partitioned into a plurality of banks, each bank including at least one register and at least one clock input, address input and data input.

The enable logic is configured to selectively disable at least one unused bank from among the plurality of banks by gating off the clock, address and data inputs thereof.

According to another example embodiment and as generally consistent with claim 15, a method of controlling power dissipation in a register file involves receiving first and second enable signals respectively directed to first and second banks of registers among a plurality of banks of registers in the register file. Each bank of registers includes at least one register and at least one clock input, address input, and data input. The first bank of registers is selectively disabled in response to the first enable signal by gating off the clock, address and data inputs thereof. See, for example, FIG. 1 and FIG. 2 and related discussion at paragraphs 0037-0038.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection are listed below.

1. Whether the rejection of claims 1-7, 12-13 and 15-19 under 35 U.S.C. § 103(a) over Garg, *et al.* (US Patent 5,493,687) in view of Boice, *et al.* (U.S. Patent No. 6,301,671) is proper.

2. Whether the rejection of claims 8-10 and 20-21 under 35 U.S.C. § 103(a) over the '687 and '671 references, and further in view of Gupta, *et al.* (U.S. Patent No. 5,996,083), is proper.

VII. Argument

Appellant notes that claim 11 is understood to be allowable because the Final Office Action removed the previous (and only remaining) rejection thereof. Appellant also understands that claim 14 is allowable in view of the Amendment filed on June 13, 2008, which amended the claim to read "a transmission medium in a computer" and thus falls under statutory subject matter, consistent with the Examiner's indications. In this regard, Appellant understands that claims 1-10, 12-13 and 15-21 stand for appeal.

All of the claim rejections must be reversed because each rejection relies upon a cited combination of references that does not provide correspondence to the claim limitations; the Office Actions of record have, to date, failed to cite a combination of references that teaches or suggests all of the claimed limitations despite Appellant's

arguments pointing out this lack of teaching. Moreover, the alleged motivation for combining the cited references lacks any evidentiary support or explanation as to how the alleged technical result would be realized. The following more particularly address these matters in connection with the above grounds of rejection.

1. The rejection of claims 1-7, 12-13 and 15-19 under 35 U.S.C. § 103(a) over Garg, *et al.* (US Patent 5,493,687) in view of Boice, *et al.* (U.S. Patent No. 6,301,671) must be reversed because the cited combination of references does not teach or suggest all of the claim limitations and because there is no motivation to combine the references.

A. The Section 103 rejection of claims 1-7, 12-13 and 15-19 must be reversed because the cited combination of references does not teach or suggest all of the claim limitations.

The cited portions of the '671 reference do not disclose claim limitations directed to selectively disabling an unused register bank by gating off each of clock inputs, address inputs and data inputs, instead saving power by selectively controlling register updates to active memory. The cited power savings approach in the '671 reference is thus fundamentally different from the claimed invention because the '671 reference involves controlling an actively-used memory array and does not, as claimed, involve disabling an unused bank. As relevant to the rejection of independent claims 1 and 15, the Final Office Action cites to two different portions of the '671 reference (*e.g.*, the first relating to FIG. 7(a/b) and the second to FIG. 8, but has mischaracterized the teachings related to these figures in attempting to show correspondence to the claimed invention. Each of these cited portions achieves power savings by respectively selectively clocking an on-chip array and by selectively updating a register in an active memory arrangement. However, neither of these cited portions, alone or in combination, provide correspondence to each of the claim limitations directed to gating off clock, address and data inputs to selectively disable unused banks (*see, e.g.*, claim 1 or 15), and the cited operations in the '671 reference are not applicable to controlling an unused register bank. The Final Office Action has thus not cited portions of the '671 reference as providing respective correspondence to each of the (three) clock, address and data inputs, and the Advisory Action's reference to these alleged teachings similarly lack any specific citation to teachings of each and every one of these limitations, as applicable to all of the claims.

Referring to FIG. 7(a) and corresponding description at column 10:17-34 in the '671 reference, a logic signal transitions the clock of an on-chip array 200 "only when needed" to serve its power-saving purpose. Referring to FIG. 8 and corresponding description at column 10:43-67 of the '671 reference, register updates are selectively controlled using control signals 210 and 212 (*i.e.*, to select whether the values stored in address/data register 209 should be updated or hold their previous values). In this regard, the approaches shown in and described in connection with FIG. 7(a) and FIG. 8 control updates to occur in active registers, and further control these updates to occur only when a register value changes in order to save power. These cited portions of the '671 reference do not involve any "gating off" as suggested in the Final Office Action and such "gating off" is both unnecessary and inapplicable (because inputs are only applied when needed, and because the cited register is active and not turned off). Moreover, the cited portions in FIG. 8 relating to selective address and data input control work to save power regardless of the clock input; the clock input for such operation is free-running and continually applied (*i.e.,* oscillator signal 11 for address/data register 209 is not gated off). In this context, the power-saving approach of the '671 reference involves an active register and is wholly different from claim limitations directed to gating off clock, address and data inputs in order to disable an unused bank, as well as limitations related thereto.

The Final Office Action has also failed to show correspondence to various other limitations in one or more dependent claims. For example, regarding claims 6 and 18, cited column 10:19-22 of the '671 reference does not disclose enable logic that determines when the array is unused as asserted. This claimed approach is useful, for example, for dynamically monitoring a plurality of banks in order to turn off unused banks. As discussed above, the '671 reference does not disclose disabling an entire register bank, and is instead directed to controlling the update of an actively-used memory. Applicant has reviewed this cited portion as well as other portions of the '671 reference and cannot ascertain any disclosure of limitations directed to either disabling a bank or dynamically determining "which register banks are unused." In this regard, the rejections of claims 6 and 18 must also be reversed for these reasons, in addition to those discussed above in connection with the independent claims. Accordingly, the rejection of

claims 7 (which depends from claim 6) and 19 (which depends from claim 18) should also be reversed.

In view of the above, the '671 reference's power savings purpose involves either controlling the transition of a clock or controlling the update of a register, thus failing to provide correspondence to disabling an unused register bank by gating off of all three of clock, address and data inputs. In summary, the '671 reference is wholly unrelated to the claim limitations against which the Final Office Action has asserted the '671 reference. The Final Office Action has accordingly failed to show any teaching or suggestion of limitations directed to gating off all three of clock, address and data inputs to a register (or otherwise). The Section 103(a) rejection of claims 1-7, 12, 13, and 15-19 is therefore improper and must be reversed.

B. The Section 103 rejection of claims 1-7, 12, 13, and 15-19 must be reversed because the asserted motivation is unsupported by any evidence from the prior art.

The motivation alleged in the Final Office Action relies upon a prediction that is unsupported by any reference from the prior art and that lacks relevance to the primary reference and its intended purpose. As asserted at pages 4 and 5 of the Final Office Action, the Examiner predicts that "gating the clock, address and data signals of Garg's [the '687 reference] register bank would prevent unnecessary signal transitions in the register bank, thus providing the benefit of reducing power dissipation." However, the Final Office Action is silent as to any description as to why this prediction would be applicable to the '687 reference, and offers no evidence of motivation for modifying the reference as suggested. Instead, the Final Office Action cites portions of the secondary '671 reference that are directed to "obviating unnecessary internal array node transitions" for power reduction in a video encoder device. The Examiner has not indicated, and the Appellant cannot ascertain, any discussion of issues relating to "unnecessary internal array node transitions" in the '687 reference's RISC microprocessor or that the microprocessor is susceptible to any internal array node transitions that would benefit from the proposed combination of references. The Advisory Action similarly fails in concluding that "[i]t would have been obvious to one of ordinary skill in the art that

Boice's [the '671 reference] teachings could have been applied to Garg, with the predictable result that gating the input signals to Garg would have produced a decrease in power consumption." To date, the Examiner has provided no citation in support of this alleged "predictable result" and, as discussed above, Appellant cannot ascertain any discussion of issues in the '687 reference relating to this purported motivation. In this regard, the rejection has failed to allege motivation relevant to the '687 reference, or provide evidence of such motivation; therefore, the Section 103 rejection must be reversed.

2. The rejection of claims 8-10 and 20-21 under 35 U.S.C. § 103(a) over the '687 and '671 references, and further in view of Gupta, *et al.* (U.S. Patent No. 5,996,083) must also be reversed because the cited references do not teach or suggest all of the claim limitations, and because there is no motivation to modify the references.

The Section 103(a) rejection of claims 8-10, 20 and 21 must be reversed because the cited combination of references does not correspond to the claimed invention. This is consistent with the above discussion in issue 1, for which reasons the rejections of independent claims 1 and 15 should be reversed and which are fully incorporated here. In at least this regard, the rejection of claims 8-10, 20 and 21 is improper because these claims depend from either claim 1 or claim 15 (if an independent claim is nonobvious under 35 U.S.C.§ 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)). Therefore, the Section 103(a) rejection of claims 8-10, 20 and 21 must also be reversed.

Appellant submits that rejections of claims 8-10, 20 and 21 are also improper because the cited combinations of references does not result in a combination that provides correspondence to claim limitations directed to providing enable signals to a register bank (*e.g.*, to turn the bank on), because the 671 reference involves active memory that is already "on." As discussed above (in 1), the selective application and control in the '671 reference involves controlling the update of an active register (*see, e.g.*, column 10:43-67 of the '671 reference). In this regard, the proposed combination of the cited power control register of the '083 reference to the active memory in the '671

reference does not provide correspondence to the claimed invention as suggested in the Final Office Action.

In addition to the above, Appellant submits that there is no motivation to combine the asserted power state and/or mode approaches in the '083 reference with the '671 and 687 references in order to arrive at the claimed invention because the cited active memory control in the '671 reference does not involve disabling a register bank. As described above, the '671 reference involves actively controlling memory that is currently being used (*see* FIG. 7(a) and FIG. 8). In this context, the alleged motivation for "providing the ability to predict when a given functional block would be needed" is thus not relevant to the active control of memory as discussed in the '671 reference.

In view of the above, the rejections of claims 8-10, 20 and 21 are improper because the rejections of corresponding independent claims 1 and 15 are improper, and further because the proposed combination of references fails to disclose all of the claim limitations and is unmotivated. In this regard, there is no *prima facie* case of obviousness and the Section 103 rejections of claims 8-10, 20 and 21 must be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-21 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/561,627)

1. A circuit arrangement comprising: (a) a register file partitioned into a plurality of banks each bank including at least one register and at least one clock input, address input and data input; and (b) enable logic coupled to the register file and configured to selectively disable at least one unused bank from among the plurality of banks by gating off the clock, address and data inputs thereof.

2. The circuit arrangement of claim 1, wherein the each register in the register file comprises at least one of a CMOS flip flop and a CMOS latch.

3. The circuit arrangement of claim 1, wherein the enable logic comprises a plurality of enable circuits each enable circuit coupled to a register bank in the register file, and each enable circuit configured to gate off each clock, address and data input supplied to the associated bank in response to a respective enable signal.

4. The circuit arrangement of claim 3, wherein each enable circuit includes a plurality of gate transistors, each gate transistor coupled to one of the clock, address and data inputs, and each gate transistor responsive to the respective enable signal supplied to each enable circuit.

5. The circuit arrangement of claim 1, further comprising output select logic coupled to each of the plurality of banks of registers.

6. The circuit arrangement of claim 1, wherein the enable logic is configured to dynamically determine which register banks are unused and to generate an enable signal for each bank in response to the dynamic determination.

7. The circuit arrangement of claim 6, wherein the enable logic comprises an address decoder configured to generate the enable signals responsive to at least one address specified by the address inputs supplied to the register file.

8. The circuit arrangement of claim 1, wherein the enable logic is configured to generate an enable signal for each bank in response to stored power modes state information.

9. The circuit arrangement of claim 8, further comprising a support register configured to store the power modes state information, wherein the support register is configured to be updated responsive to a power control instruction resident in program code being executed by a processor.

10. The circuit arrangement of claim 9, wherein the support register comprises a power modes register.

11. The circuit arrangement of claim 9, wherein the support register additionally stores status information that is unrelated to power dissipation control.

12. The circuit arrangement of claim 1, wherein the circuit arrangement is disposed on an integrated circuit.

13. The circuit arrangement of claim 12, wherein the circuit arrangement is disposed in a processor in the integrated circuit.

14. A program product comprising a hardware definition program defining the circuit arrangement of claim 1, and a signal bearing medium bearing the hardware definition program, wherein the signal bearing medium includes at least one of a transmission medium in a computer and a recordable medium.

15. A method of controlling power dissipation in a register file, the method comprising: (a) receiving first and second enable signals respectively directed to first and second banks of registers among a plurality of banks of registers in the register file, wherein each bank of registers includes at least one register and at least one clock input, address input, and data input; and (b) selectively disabling the first bank of registers responsive to the first enable signal by gating off the clock, address and data inputs thereof.

16. The method of claim 15, wherein the each register in the register file comprises at least one of a CMOS flip flop and a CMOS latch.

17. The method of claim 15, wherein selectively disabling the first bank of registers includes supplying the enable signal to a plurality of gate transistors coupled to the first bank of registers, each gate transistor coupled to one of the clock, address and data inputs.

18. The method of claim 15, further comprising dynamically determining that the first bank is unused, and generating the first enable signal responsive thereto.

19. The method of claim 18, wherein dynamically determining that the first bank of registers is unused includes decoding at least one address specified by the address inputs supplied to the register file.

20. The method of claim 15, further comprising generating the first and second enable signals in response to stored power modes state information.

21. The method of claim 20, wherein the stored power modes state information is stored in a support register, the method further comprising updating the support register in response to a power control instruction resident in program code being executed by a processor.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.